HARDWARE DESCRIPTION OF THE EXPANSION BOX

The box consists of two main elements, the Buffer Box and the Expansion Box Chassis. This document will concern itself with the hardware inside the Expansion Box Chassis as the Buffer Box is a simple signal buffer unit. The Expansion Chassis contains a backplane, for option connection, a power supply and I/O channels.

The I/O channels consist of two serial RS232C channels and one Centronics type parallel output port. These functions are created by two 68B50 ACIAs, one 68B21 PIA, and a BR1943 baud rate generator. Figure 1 shows the locations of the devices in the memory map. All the devices respond to Parallel Bus Device #6.

Location	Device
D100H	68B50 Channel A
D104H	68B50 Channel B
D108H	68B21
D110H	1943

Figure 1

Parallel Channel Description

The Parallel channel uses a 68B21 PIA. There are 11 signals implemented in the Centronics Interface. These signals are D0-D7, Data Strobe, Busy, and Fault. The data lines use port A in the PIA and are output only. Data Strobe is an output line from port B bit 4 which is used to strobe data to the printer. This signal should be active after data is stable and the printer is not busy. Busy is an input line of port B bit 5. This input controls the flow of data to the printer; it should be checked before next data transmission. Fault is an input of port B bit 6. This input indicates if the printer had a fault (ie. paper out) and should always be checked. Figure 2 shows the port assignments for the PIA. The register types and control bits are the same as the standard Atari PIA used in current computers.

Port	Direction	Description
A0	Output	Data Bit 0
A1	Output	Data Bit 1
A2	Output	Data Bit 2
A3	Output	Data Bit 3
A4	Output	Data Bit 4
A5	Output	Data Bit 5
A6	Output	Data Bit 6
A7	Output	Data Bit 7

B0	Input	DSR' Channel A
B1	Output	DTR' Channel A
B2	Output	DTR' Channel B
B3	Input	DSR' Channel B
B4	Output	Data Strobe'
B5	Input	Busy'
B6	Input	Fault'
B7	Not Used	Not Used

Figure 2
Baud Rate Selection

The baud rate for the two serial channels is created by a BR1943 baud rate generator. This device creates two different baud rates using one write only register. The upper four bits of this register controls the baud rate for Channel B, the lower four bits control Channel A. Figure 3 shows the four bit combinations for the 16 different baud rates.

Sel Value	Baud Rate
0000	50
0001	75
0010	110
0011	134.5
0100	150
0101	200
0110	300
0111	600
1000	1200
1001	1800
1010	2400
1011	3600
1100	4800
1101	7200
1110	9600
1111	19200

Figure 3

Serial Channels

The two serial channels are a full RS-232C type. These channels use the baud rates from above, handshake internal to the ACIA as well as extra handshake lines from the PIA. The ACIA operation is described below as well as register locations. The software should provide correct operation of the extra handshake lines for full modem control.

ACIA REGISTERS DESCRIPTION

The ACIA has internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 1.

Data Bus #	Transmit Data Register	Receive Data Register	Control Register	Status Register
0	Data 0	Data 0	C D Sel 1 CRO	RDRF
1	Data 1	Data 1	C D Sel 2 CR1	TDRE
2	Data 2	Data 2	Word Sel 1 CR2	DCD'
3	Data 3	Data 3	Word Sel 2 CR3	CTS'
4	Data 4	Data 4	Word Sel 3 CR4	Frame Error
5	Data 5	Data 5	Transmit Con 1 CR5	Receiver Overrun
6	Data 6	Data 6	Transmit Con 2 CR6	Parity Error
7	Data 7	Data 7	Rec Int En CR7	Interrupt Request

Table 1
Definition of ACIA Register Contents

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the ACIA has been addressed and RS . R/W is selected. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receive Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status register.

CONTROL REGISTER

The ACIA Control Register consists of eight bits of write-only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) - The counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the

transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a master reset for the ACIA which clears the Status Register (except for external conditions on CTS and DCD) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	Divide by 1
0	1	Divide by 16
1	0	Divide by 64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) - The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits Even Parity 2 Stop Bits
0	0	1	7 Bits Odd Parity 2 Stop Bits
0	1	0	7 Bits Even Parity 1 Stop Bit
0	1	1	7 Bits Odd Parity 1 Stop Bit
1	0	0	8 Bits 2 Stop Bits
1	0	1	8 Bits 1 Stop Bit
1	1	0	8 Bits Even Parity 1 Stop Bit
1	1	1	8 Bits Odd Parity 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) - Two Transmitter Control bits provide for the control of the interrupt from the Transmit data Register Empty condition, the Request-to-Send (RTS) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	RTS'=LOW Trans INT Disabled
0	1	RTS'=LOW Trans INT Enabled
1	0	RTS'=HIGH Trans INT Disabled
1	1	RTS'=LOW Trans a BREAK CHAR

Receive Interrupt Enable Bit (CR7) - The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7): Receive Data Register Full, Overrun, or a low to high transition on the Data Carrier Detect (DCD) signal line.

STATUS REGISTER

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit 0 - Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 - The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect (DCD), Bit 2 - The Data Carrier Detect bit will be high when the DCD input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains high after the DCD input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the DCD input remains high after read status and read data or master reset has occured, the interrupt is cleared, the DCD status bit remains high and will follow the DCD input.

Clear-to-Send (CTS), Bit 3 - The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low CTS indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send Status bit.

Framing Error (FE), Bit 4 - Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 - Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent

characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 - The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request (IRQ), Bit 7 - The IRQ bit indicates the state of the IRQ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the IRQ output is low the IRQ bit will be high to indicate the interrupt or service request status. IRQ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

Expansion Box Specifications
7/27/83

1.0 Introduction

The Expansion Box will be a buffered extension of the Parallel Bus Interface (P.B.I.) allowing system expansion and enhancement. The bus will enable the consumer to connect a variety of different devices to the Parallel Bus Interface. Some future devices are listed below.

1) Disk Drive Controller-*
2) Votrax-
3) Modem (300 and/or 1200)-*
4) Touch Tone Decoder-
5) EPROM Programmer-
6) B.S.R. Controller Interface-
7) Relay Switch Card-
8) IEEE 488 Control Card-*
9) Real Time Clock-
10) 80 Column Display-*
11) Printer Spooler/Buffer-
12) APPLE Card-*
13) VCS Adapter Card-*
14) A/D Converter Card-*
15) Infra Red Interface-*
16) Hard Disk Interface-*
17) Music Card-
18) Speech Recognition-*
19) Ram Disk-*

20) Battery Back-up CMOS RAM-
21) Corvus Interface-*
22) Ethernet Interface-*
* indicates a smart device.

1.1 Product Objectives

A. To provide future system expansion.
B. To provide multiple device access to the P.B.I.
C. To provide an interface standard to envoke interest from peripheral manufacturers in developing P.B.I. Devices.

1.2 References

Sweet 16 Expansion Box Specification, A. Chopra
P.B.I. Specification, S. Miller
SURELY O.S. Rom Specification, S. Scheiman R. Nordin
Software Implementation of Parallel Devices, R. Nordin

2.0 Product Description

The Expansion Box will provide two RS-232C Serial Channels and one Centronics type Parallel Output Port in addition to eight (8) expansion slots. The connection to the XL-Series computer is made through the Parallel Bus Interface. Devices that plug into the P.B.I. are called Parallel Bus Devices (P.B.D.). The Expansion Box is a P.B.D.. The Interface in the Expansion Box to the expansion devices is called the Expansion Box Interface (E.B.I.). Modules that plug into the expansion slots will be called Expansion Box Devices (E.B.D.).

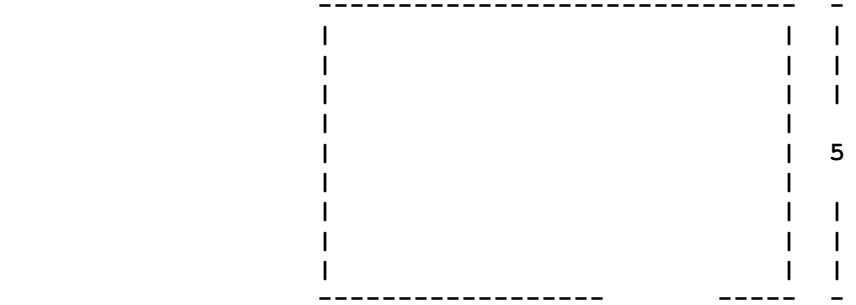
2.1 Mechanical

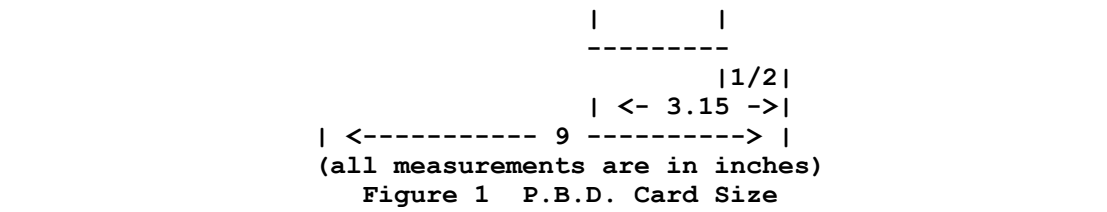
2.1.1 Appearance

The Expansion Box should match the styling of the current XL product line. The Box should have all connections from devices, power, and bus signals in the rear of the box. The power switch and power indicator light should be placed on the front panel.

2.2.2 Design Concepts

The Expansion Box should not require more than one square foot of table space. It should also be able to support a 13 inch color television. The top must be easily removable so the user can access the option cards, but not be able to access the power supply or come in contact with the Line Voltage. The Box will support eight 9 by 5 inch option cards (see figure 1).





(all measurements are in inches)

Figure 1 P.B.D. Card Size

2.2 Electrical

2.2.1 Expansion Box Interface

The E.B.I. contains all the signals in the P.B.I. plus power for the E.B.D.. The description of the E.B.I. in this document is similar to that of the P.B.I. but note the differences in timing and loading.

2.2.1.1 Connector

The Expansion Box Interface signals will be accessible through a 50-pin connector. This connector is an AMP type 67987-4. It will mate to a standard card edge with gold plated fingers at .100 inch centers.

EXTSEL'	2	1	GND
A1	4	3	A0
A3	6	5	A2
A5	8	7	A4
GND	10	9	A6
A8	12	11	A7
A10	14	13	A9
A12	16	15	A11
A14	18	17	A13
A15	20	19	GND
D1	22	21	D0
D3	24	23	D2
D5	26	25	D4
D7	28	27	D6
GND	30	29	GND
GND	32	31	B02
RST'	34	33	+5 VDC
RDY	36	35	IRQ'
EXTENB'	38	37	-12 VDC
REF'	40	39	+12 VDC
GND	42	41	CAS'
RAS'	44	43	MPD'
LR/W'	46	45	GND
+5 VDC	48	47	+5 VDC
GND	50	49	AUDIO

Figure 2 Expansion Socket

2.2.1.2 Signals

Shown in Figure 2 is the pin-out of the connector looking into the expansion box. The signal pin numbers and signal names are described below.

Pin 2 EXTSEL' External Select (Input) ==> This open collector line is generated internally by the Expansion Box Device (E.B.D.). This signal should be active low whenever EXTENB is active and the E.B.D. is selected and there is a valid E.B.D. address on the bus. EXTSEL' causes a CAS' inhibit on the main board allowing a remapping process. Although an E.B.D. can be mapped in any VALID RAM location, these devices should follow the ATARI guidelines for E.B.D. locations so future ATARI devices can be used. The drive device should be capable of sinking 10mA.

Pin 3 A0 Address Line 0 (Output) ==> Address line 0 is a buffered output from the microprocessor.

Pin 4 A1 Address Line 1. Same as above.
Pin 5 A2 Address Line 2. Same as above.
Pin 6 A3 Address Line 3. Same as above.
Pin 7 A4 Address Line 4. Same as above.
Pin 8 A5 Address Line 5. Same as above.
Pin 9 A6 Address Line 6. Same as above.
Pin 11 A7 Address Line 7. Same as above.
Pin 12 A8 Address Line 8. Same as above.
Pin 13 A9 Address Line 9. Same as above.
Pin 14 A10 Address Line 10. Same as above.
Pin 15 A11 Address Line 11. Same as above.
Pin 16 A12 Address Line 12. Same as above.
Pin 17 A13 Address Line 13. Same as above.
Pin 18 A14 Address Line 14. Same as above.
Pin 20 A15 Address Line 15. Same as above.

Pin 21 D0 Data Line 0 (Bi-directional) ==> Data line 0 is a buffered bi-directional data line.

Pin 22 D1 Data Line 1. Same as above.
Pin 23 D2 Data Line 2. Same as above.
Pin 24 D3 Data Line 3. Same as above.

Pin 25 D4 Data Line 4. Same as above.
Pin 26 D5 Data Line 5. Same as above.
Pin 27 D6 Data Line 6. same as above.
Pin 28 D7 Data Line 7. Same as above.

Pin 31 B02 Buffered Phase 2 Clock (Output) ==> This clock output line is a buffered phase 2 clock from the processor.

Pin 34 RST' Reset (Output) ==> Reset is an active low signal which occurs either on power-up or by depressing the reset key on the computer.

Pin 35 IRQ' Interrupt Request (Input) ==> This open collector line creates an interrupt on the microprocessor. The interrupt can then invoke the handler ROM or other service routines for the E.B.D.. The driving device should be capable of sinking 10mA.

Pin 36 RDY Ready (Input) ==> This open collector input signal allows the E.B.D. to halt the microprocessor ONLY during read cycles. This will extend the read cycle for slow peripherals. The driving device should be capable of sinking 10mA.

Pin 38 EXTENB External Decoder Enable (Output) ==> This output goes high when there is a valid ram access. Any E.B.D. can map during a valid EXTENB but the E.B.D. should only map in according to ATARI specified address locations.

Pin 40 REF' Refresh (Output) ==> This output can be for refresh timing on volatile memories connected to the E.B.I..

Pin 41 CAS' Column Address Strobe (Output) ==> This output can be used for access of DRAM external to the computer. Due to timing restrictions caution should be taken when using this signal in the expansion box.

Pin 43 MPD' Math Pack Disable (Input) ==> This open collector input is used to disable the math pack section of the OS ROM (D800H-DFFFH). This should be done when the E.B.D. is selected and has a handler resident. The driving device should be capable of sinking 10mA.

Pin 44 RAS' Row Address Strobe (Output) ==> This output can be used for access of DRAM external to the computer. Due to timing restrictions caution should be taken when using this signal in the expansion box.

Pin 46 LR/W' Latched Read Write (Output) ==> This output is active high for a read cycle and active low for a write cycle.

Pin 49 AUDIO Audio In (Input) ==> This line is tied directly to the audio summation network of the computer. The audio signal input is 100 mV peak to peak with 4.7K ohm source impedance.

Pins 1,10,19,29,30,32,42,45,50 are Ground (GND).

Pins 33,47,48 are +5 Volts.

Pin 37 is -12 Volts.

Pin 39 is +12 Volts.

2.2.1.3 Interface Requirements

For peripherals to interface through the E.B.I. to the computer the following requirements must be followed.

2.2.1.3.1 D.C. Characteristics

All E.B.I. outputs from the Buffer Box have the capability of driving TTL load.

All E.B.I. open collector input lines must be able to sink 10mA (min) at .4V (max).

All E.B.I. non-open collector input lines except AUDIO must have the drive capability of 48mA at logic 0 (Iol) and -15mA at logic 1 (Ioh).

All E.B.I. signals except AUDIO will be at standard TTL logic levels.

The AUDIO input line must drive a 4.7K Ohm source impedance with a 100mV peak to peak signal.

2.2.1.4 Hardware Device Protocol

The E.B.I. is designed to support two types of devices. The first is an Expansion Box Peripheral (E.B.P.) and the second is an External Application Cartridge (E.A.C.).

2.2.1.4.1 Expansion Bus Peripherals (E.B.P.)

The E.B.P.s have the following characteristics:

1. The interface between the E.B.P. and the CPU is defined through the handler/OS resident in the OS ROM. The OS can support 8 devices at one time with only one enabled during any given interval.

2. Every E.B.P. has a unique handler that resides in the CPU memory from D800H-DFFFH. The ROMS containing the code for these handlers are physically resident on the respective E.B.P.s. To access this handler, the math pack must be disabled with MPD'. When the math pack is disabled (this should happen whenever the E.B.P. is selected and has an external handler) the computer will generate EXTENB for the math pack area. The E.B.P. must generate the correct EXTENB/EXTSEL' protocol. If the device does not generate EXTSEL' the CPU will access (in the 64K computers) an unused area of ram. This area should not be used since all computers of this series do not have that area of ram.

3. The location D1FFH in the CPU memory map is reserved for passing control information between the CPU and the E.B.P.s. The CPU selects one of the E.B.P. devices by writing a "1" into the desired bit in location D1FFH. The device can be deselected by writing a "0" into the desired bit.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Therefore the CPU can then access 8 devices, one at a time. If the IRQ' line is pulled "low" the CPU can read the status for location D1FFH and locate the requesting E.B.P.. A "1" in a bit Ix (where x=0 to 7) corresponds to an interrupt in E.B.P. x. If the bit is a "0" then the device has not caused the interrupt. The E.B.P. must clear the interrupt flag when the interrupt is being serviced.

7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0

4. An E.B.P. should assert MPD' only when it is selected. An E.B.P. should assert EXTSEL' only when it is selected and if EXTENB' is asserted.

5. An E.B.P. may respond to any selects D0 through D7. It is recommended that the E.B.P.s have configuration switches to allow them to respond to any one of the selects. Some of the computer systems use the E.B.I. to support internal devices therefore the user should check each manual for device locations. If the system has devices in specific locations, those are reserved in that computer.

6. An E.B.P. handler may respond to addresses in the region D800H-DFFFH only when it is selected.

7. A peripheral may respond to addresses in the region D100H to D1FEH only when selected.
8. The E.B.P.s will have software priority over the SIO peripheral when they are addressed generically.

9. Data transfer between the CPU and the E.B.P. is under the control of the peripheral handler for the E.B.P.s. The peripheral handler may or may not be in the E.B.P. Data transfer is handled by a combination of code in the O.S. and the E.B.P.
10. The E.B.P.s shall work if a cartridge is present in the cartridge slot.
11. The CPU address space from D600H to D7FFH is reserved for E.B.I. devices as follows:

Device	Range	Size
D0	D600H-D61FH	32 Bytes
D1	D620H-D63FH	32 Bytes
D2	D640H-D65FH	32 Bytes
D3	D660H-D67FH	32 Bytes
D4	D680H-D69FH	32 Bytes
D5	D6A0H-D6BFH	32 Bytes
D6	D6C0H-D6DFH	32 Bytes
D7	D6E0H-D6FFH	32 Bytes

The region from D700H to D7FFH is reserved for use by ATARI. The CPU address space from D600H to D7FFH is always mapped to the E.B.I. and does not require the EXTENB/EXTSEL' protocol. Some units may have devices mapped on the E.B.I.; these devices are only active when selected but care must be taken when using a unit with onboard devices.

2.2.1.4.2 External Application Cartridges

The "External Application Cartridge" (EAC) is a generalization of the E.B.P.. They have the following characteristics:
1. An EAC can reside at any or all of the locations in the region 0000H to BFFFH for which the EXTENB is generated. They may respond to these addresses only when "opened".
2. The EACs must be opened by the protocol given for the E.B.P.s.
3. The EACs must conform to the EXTENB/EXTSEL' protocol.
4. The EACs must have a handler (resident at location D800H-DFFFH) that controls their operation. The EACs must conform to conditions (4) through (11) of section III. B. above.
5. The EACs will work if a cartridge is present in the internal cartridge slot.

2.2.2 I/O Channels

The expansion box contains two RS-232C serial channels and one Centronics type parallel printer channel. Both the serial and parallel channels are preset to device #6. This device cannot be used in the Expansion Box.

2.2.2.1 Serial Channel Description

The Expansion Box will have two RS-232C Asynchronous serial channels capable of simultaneous two way communication. Both channels should be addressable through software via CIO using the same format as the serial channels in the ATARI 850. The baud rate will be software selectable from 16 baud rates (see Table 1). The baud rates of the two channels are to be independent of each other.

Sel Value	Baud Rate
0000	50
0001	75
0010	110
0011	134.5
0100	150
0101	200
0110	300
0111	600
1000	1200
1001	1800
1010	2400
1011	3600
1100	4800
1101	7200
1110	9600
1111	19200

Table 1 Baud Rate Selection Chart

2.2.2.2 Parallel Channel Description

The basic Parallel Channel is to support a Centronics type parallel printer. To do this the following signals are supported.

D0-D7	Data Lines
DS'	Data Strobe
BUSY	Busy Input
FA'	Fault Input

2.2.3 Buffer Box

To allow connection to the XL-series computer, the Expansion Box will use a buffer box connected to the back of the computer. This Buffer Box will be able to drive a 3 foot long cable and the Expansion Box. The power used by the Buffer Box will be supplied by the Expansion Box on the Reserved Pins of the cable. The connectors used will be the standard 50 pin P.B.I. connectors.

2.2.4 Power Supply

The Expansion Box power supply will have sufficient output to drive each slot with .75 Amps at +5 VDC, .1 Amps at +12 VDC, and .1 Amps at -12 VDC. Table 2 shows max operating current limits of the supply. A fan might be necessary to provide cooling in the Expansion Box.

+5 VDC	6.75 Amps
+12 VDC	1.0 Amps
-12 VDC	1.0 Amps

Table 2

2.3 Software

2.3.1 Expansion Bus Protocol

The Software handlers and application programs written for use with/in the Expansion Box must follow standard Protocol defined by "The Software Implementation of Parallel Device Handlers and Drivers" by Rick Nordin. A Designers guide to interfacing devices to the PBI and Expansion Box will also contain the required documentation concerning the protocol.

2.3.2 I/O Channel Handlers

The handler used in the Expansion Box I/O channel will conform to the above specifications as well as providing support for the printer as a standard CIO device call.

2.4 Product Performance

This section will specify the projected performance of the Expansion Box. The environmental and reliability information that is included is targeted from the Sweet 16 specification.

2.4.1 Environmental

Operating Environment
Temperature =
Maximum: 45 degrees C
Minimum: 10 degrees C
Humidity =
Maximum: 90% R.H. (Non Condensing)
Minimum: 15% R.H.
Altitude =
Maximum: 3000 Meters (9840 feet) (720 millibars)
Minimum: -60 Meters (-197 feet) below sea level

Non-Operating Environment
Temperature =
Maximum: 60 degrees C
Minimum: -30 degrees C
Humidity =
Maximum: 90% R.H.
Minimum: 0% R.H.
Should condensing occur, unit must be dried off before operation.

Altitude = Same as operating

2.4.2 Endurance Levels

ESD Susceptibility
No product damage or data loss with 10 KV to 20 KV discharge at any point accessible to the user except the connectors.

Vibration
Operation: .1g +- 10% 5 to 500Hz
Resonance Search: Sine scan 5-100 Hz dwell on resonances 1.0g for 10 minutes.

Transportation: 100 to 300 cycles per minute 2 directions 90 degrees apart, 30 minutes; each frequency to be such as to raise package from the table 0.06 in., acceleration to be 1.0g (min) No Damage should result.

Impact Test: Free fall distance of 24 in. on corner, edge, and all 6 faces. No damage should occur to a packed unit.

Random Vibration: 0.04g 2Hz 15 minutes; 10 to 1000Hz 6.3g RMS

Thermal Shock: 10 degrees C for 3 hours power on raise temperature, 5 degrees per minute to 45 degrees C for 5 hours power off drop temperature 5 degrees C per minute to 10 degrees C. Repeat cycle 5 times no damage

2.4.3 MTBF & MTTR
The targeted MTBF for the Expansion Box is 8000 hours continuous power-on at 25 degrees C.
The targeted MTTR for the unit is 5 minutes.

2.4.4 Compliances
UL 114 & UL 94HB
CSA C22.2 No. 154
FCC Docket 20780, Part 15, Subpart J, Class B

Expansion Box Specifications
10/14/83

Below are the changes to the document of the same name dated 7/27/83.

1.2 Assumptions

1.2.1 Product Reasoning
This product is intended to add a strategic marketing dimension to the Atari home computer line by providing expansion capability.

1.2.2 Manufacturing

It is assumed that the Expansion Box will be manufactured by some, as yet unspecified, overseas vendor.

1.2.3 Strategic Fit

This product is intended to broaden Atari's image as a complete computer supplier. This is done by offering an expansion path for computer users to grow with their systems. A line of option cards will allow even the most sophisticated users to advance to an advanced system.

1.2.4 Product History

As of the date of this document the expansion box has been redefined as a smart device rather than an extension of the Parallel Interface Bus. This was done to facilitate third party vendors in the implementation of option cards. This will also allow for easy interfacing of the Expansion Box to the current 400/800 installed base. This choice should create added sales of this device as well as showing the public Atari will not leave current users unsupported! In addition to the above features, a RFI problem is also reduced creating a faster path to bring the product to market.

1.3 References

Sweet 16 Expansion Box Specification, A. Chopra
P.B.I. Specification, S. Miller
SURELY O.S. Rom Specification, S. Scheiman, R. Nordin
Software Implementation of Parallel Devices, R. Nordin
Sweetpea Product Specification, D. Lang
JULIE FIFO Specification, S. Miller

2.2.2.4 Hardware Device Protocol

The hardware protocol for the Expansion Box is similar to the Expansion Bus Interface on the computer in that each card is selected through a common register. There will also be device handlers on each card in a fixed location of memory. The bus timing is configured so any type of device can be easily interfaced to the Expansion Box. For complete interfacing requirements a third party vendor document will be created with examples of interfacing methods.

2.2.3 Processor Card

2.2.3.1 CPU

The CPU for the Expansion Box will use a 6502 operating at 1 MHz. This is done for software compatibility with current developmental tools. The placement of the CPU on a card allows the user to swap other CPU cards for the 6502 card.

2.2.3.2 ROM

There is provision for 8 K Bytes of monitor Rom on the processor card. This ROM can also be disabled by asserting ROMDIS' line on the bus. The ROM will be located at E000H-FFFFH.

2.2.3.3 RAM

There is provision for 2 K Bytes of general purpose RAM on the processor card. The RAM can be disabled by asserting RAMDIS' line. This will allow for remapping of page 0 and 1 to swap tasks in and out without moving large areas of memory. The RAM will be located at the bottom of the memory space.

2.2.3.4 Serial Channel Description

The processor card will have two RS-232C asynchronous serial channels, capable of simultaneous two way communication. Both channels are addressable through the CIO in the operating system of the Atari computer. The baud rates for the channels are found in table 1. Both channels have independent transmit and receive baud rates. One of the two serial ports will be jumperable to allow operation as a SIO port for operation with current Atari 400/800 units.

BAUD RATES
50
75
110
134.5
150
200
300
600
1050
1200
1800
2000
2400
4800
7200
9600
19200
38400

Table 1

2.2.3.6 Bus Interface

The Bus Interface for the processor card will support the load requirements of the Expansion Bus and follow the protocol of the Bus timing.

2.2.4 Computer Interface

The Expansion Box will interface with the Atari XL product line through an interface unit connected to the Parallel Expansion Bus. The interface unit will contain a JULIE FIFO interface chip designed to allow communications between the XL computers and the Expansion Box. In addition the interface unit will have a 2K handler rom for the P.B.I. and one LS-TTL decoder chip. Power for the interface unit will be provided by the expansion box. The Interface will be connected to

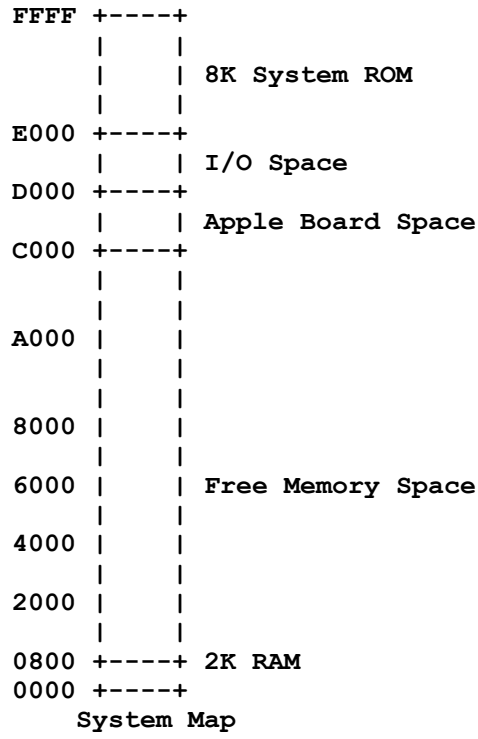
the Expansion Box via a 26 conductor double shielded cable. The cable is to be 3 feet in total length.

2.2.5 Power Supply

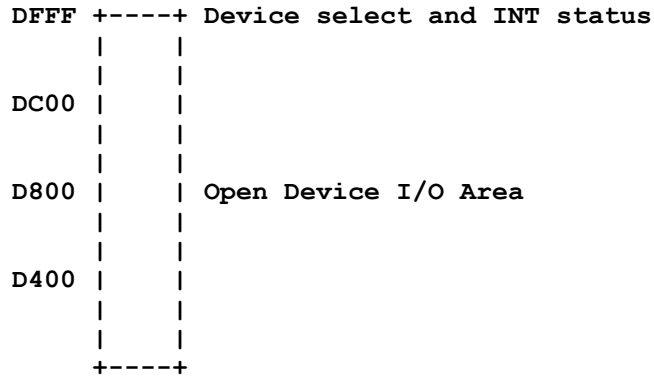
Shown below are the total power requirements.

+5 VDC	4.5 Amps
+12 VDC	0.5 Amps
-12 VDC	0.5 Amps
+9 VDC	0.2 Amps unregulated

2.2.6 Memory Map



System Map



```
     |    | CPU Interface, UART, Parallel Printer
D000 +----+
     I/O Map
```

3.0 Future Enhancements

The future enhancements include a SIO card to allow operation with the current Atari 400/800 line as well as the option cards stated in the introduction. As of this document no option cards are defined.

4.0 Cost Targets

The targeted standard cost for this unit is $125. This cost will include the processor card with 2 serial channels and the interface to the current XL product line.

5.0 Packaging

5.1 Inner Packing

The inner packing must protect the Expansion Box and accessories from 10 drops from 24 inches on any of six surfaces, three edges radiating from one corner without any internal damage. The inner packing must also protect the Expansion Box and accessories from vibrations of 30 minutes each, 2 directions 90 degrees apart, 100-300 cycles per minute. Packing must leave the surface 0.06 inches at some time, again leaving no damage.

5.2 Display Carton

The display carton should be a six sided 24 pt. SBS (white chipboard) folding carton, printed in 4 colors plus PMS877 silver, with UV or other abrasion resistance coating. All graphics will be specified by Atari.

5.3 Shrink Wrap

The fully packaged product will be shrink wrapped to prevent damage and pilferage.

5.4 Shipping Carton

The weight and type of corrugate as well as the number of products per shipping carton are to be specified by Atari.

5.5 Carton Contents

* Expansion Box Unit
* Interface Unit for XL computers
* Interface Cable

* 2 RS-232C Cables
* Processor Card
* Owners Manual and Warranty card
* Atari products catalog

5.6 Product Name
The proposed official name is "Atari Expansion Box".

6.0 Manual Requirements
The unit will include an owners manual to be specified by Atari.

Expansion Box Specifications
5/11/84

Below are the changes to the documents of the same name dated 7/27/83 and 10/14/83 respectively.

1.0 Introduction
The Expansion Box is an extension device providing support of expansion cards for the Atari Computer line. This device provides Atari systems with expansion and enhancement. The bus enables the consumer to connect a variety of different devices to the Expansion Box Interface (E.B.I.). Some devices are listed below.

1) RAM EXPANSION
2) SERIAL/PARALLEL INTERFACE
3) Z-80 PROCESSOR
4) 80-COLUMN VIDEO MONITOR INTERFACE
5) HOBBYIST PROTOTYPING CARD

2.1.1 Appearance
The Expansion Box matches the styling of the current XL product line. The Box has all connections to devices and power in the rear of the box. A flat cable (connected to the front of the box) connects the Expansion Box to all PBI-equipped computers.

2.1.2 Design Concepts
The Expansion Box requires less than one square foot of table space. The top is easily removable so the user can access the option cards. The Box supports five 9 by 5 inch option cards. To remove the top of the box, the AC adaptor must be unplugged from the box.

2.2.1 Architectural Overview
The expansion box contains a triple-output power supply providing regulated +12 volts and -12 volts and +10 volts unregulated. Also provided is a half-wave rectified AC waveform (for power-line frequency reference only) and +5 volts (for reference only).

The address bus, data bus and control lines are buffered by the expansion box and bussed to the five edge connectors provided.

2.2.2.1 Connector

The Expansion Box Interface signals are accessible through a 50-pin connector. This connector is an AMP type 2-530843-9. It mates to a standard card edge with gold plated fingers at .100 inch centers.

2.2.2.3.1 D.C. Characteristics

All E.B.I. outputs have the drive capability of 24mA at logic 0 (Iol) and -6mA at logic 1 (Ioh).

All E.B.I. open collector input lines must be able to sink 10mA (min) at .4V (max).

All E.B.I. non-open collecotr input lines except AUDIO must have the drive capability of 24mA at logic 0 (Iol) and -6mA at logic 1 (Ioh).

All E.B.I. signals except AUDIO will be at standard TTL logic levels.

The AUDIO input line must drive a 4.7KOhm source impedance with a 100mV peak to peak signal.

Each expansion box card should not load any E.B.I. output line with more than three standard TTL loads.

2.2.2.3.2 A.C. Characteristics

All specifications are referenced to the standard 2 MHz 6502 specifications.

The signal PHASE2 is the 6502 clock at the processor.

2.2.2.3.3 Materials Requirements

Contact fingers shall be plated with nickel of the low-stress type, Class II per federal specification QQ-N290A. Nickel plate thickness shall be 100 +/- 25 microinches. The nickel plating shall be overplated with gold type II (23+ karat), 15 microinches minimum (130-200 knoop hardness) or 10 microinches minimum (201 or over knoop hardness). Impurities shall not exceed .1%, not including metallic hardeners. Roughness shall be less than 50 microinches.

2.2.3 Power Supply

The power supply is comprised of an external AC adaptor capable of providing 40VA at 9.5 vAC to the Expansion Box and an internal rectifier/filter/regulator system. This system provides:

+10 vDC UNREGULATED (+40% or -15%) at .5A per card slot.
+12 vDC REGULATED (+ or - 4%) at 30mA per card slot.
-12 vDC REGULATED (+ or - 4%) at 30mA per card slot.
+5 VREF REGULATED (+ or - 4%) as a reference only.
AC - a 60 Hz reference only.

Total supply current capacity is five times the per card slot amounts.

It is recommended that the Expansion Box NOT be operated with the cover removed for safety reasons and to comply with radiated emissions standards.

3.0 Notes

3.1 RAM 64KMR

The RAM 64KMR module is designed to be used in the expansion box. However, it does not completely adhere to the E.B.I. protocol since it will allow RAM to be selected in lieu of the O/S (when used in the "1064 mode".)

3.2 RESERVED MEMORY LOCATIONS

The memory space from D100H to D1AFH is available for use by most applications. This space should be used by a device with the device select bit enabling its use. If the device select bit is not used, there is potential bus conflict between E.B.D.s. The remainder of the I/O space between D1B0H and D1FFH is mapped as follows:

D1B0H - D1C7H	Speech/Modem/Disk Registers
D1C8H - D1CEH	Atari Reserved
D1CFH	Alternate Interrupt Register (1450 only)
D1D0H - D1DFH	Audio Registers
D1E0H - D1E7H	Atari Reserved
D1E8H - D1EFH	Parallel/Serial Registers
D1F0H - D1F7H	Alternate CPU Registers
D1F8H - D1FDH	80 Column Video Registers
D1FEH	RAM Bank Select Register
D1FFH	E.B.D. Select/Interrupt Register

PARALLEL BUS INTERFACE SPECIFICATIONS

1.0 Introduction:

The Parallel Bus Interface (PBI) is provided on the S-16 to support high speed peripherals, communication devices and cartridges.

The objective of the PBI is two-fold:

(1) To provide for future system improvement and expansion of the S-16.

(2) To provide a simplified interface standard that will envoke interest from peripheral manufacturers in making peripherals for the S-16.

The physical connection of the peripherals to the S-16 is conceived of being through a unit called the "Expansion Box". Roughly, the "Expansion Box" provides a low cost, easy-to-use multiple access mechanism to the PBI. It consists of electronics necessary to implement the interface protocol between the CPU and the Parallel Bus peripherals. Further details of the Expansion box are TBD.

This document gives a logical definition of the pins on the PBI. It defines the characteristics of devices that can be supported on the PBI.

The electrical specifications of the PBI signals and the details of the PBI protocol are in the S-16 Product Specification.

2.0 THE PARALLEL BUS INTERFACE

The Parallel Bus Interface Connector is a 50 pin connector (See figure 5.2.9) with the following signals.

PIN 3 through PIN 18 are A0 through A15 respectively. These are the CPU address lines. The CPU addresses the Parallel Bus Interface devices using these lines.

PIN 19 through PIN 26 are D0 through D7 respectively. These are the processor data lines. The CPU transmits and receives data and control information from the Parallel Bus Interface devices on these lines.

PINS 35, 36, and 37: are COMM A, COMM B, and COMM C select lines respectively. The Parallel Bus Interface devices lie in the CPU memory map. Three 256 byte segments of the CPU memory map are reserved for control of the parallel bus devices. COMM A selects the segment from D600 to D6FF. COMM B selects the segment from D700 to D7FF. COMM C selects the segment from D100 to D1FF. COMM A, COMM B, and COMM C are low when active.

PIN 31 is for the Buffered Phase 2 Clock (B02) Output to the Parallel Bus Interface devices.

PINS 2, 44, 45, and 46 are not connected.

PIN 29 is the IRQ (Interrupt Request) input from the Parallel Bus Interface devices. A PBI device can pull this input low to invoke the device handler that services the parallel bus device. This input is "open drain".

PIN 32 is the Read/Write (R/W) Output to the Parallel Bus Interface devices. This line is "high" for a read cycle. It is low for a write cycle.

PIN 34 is the PoWeR ON (PWRON) Input from the Parallel Bus Interface devices. This input will allow the implementation of the "auto-wakeup" feature in future enhancements of the S-16. This signal is "low" when active.

PIN 38 is reserved for future expansion.

PIN 33 is Power on Reset (POR) ouput to the Parallel Bus Interface devices. This output resets any device so designed on power up and when the RESET key on the S-16 keyboard is hit.

PIN 49 is audio in and out signal from/to the Parallel Bus devices. This line is connected directly to the audio summation network of the S-16. This audio signal is a 1 volt peak to peak.

PIN 39 is the MODSEN (Module Sense) input from the Parallel Bus Interface Modules. This input is pulled low whenever a Parallel Bus Interface module is connected to the PBI.

PINS 47 and 48 are GROUND.

PIN 28 is External Decoder Enable (EXTENB) Output. This output goes high when an address on the CPU bus is an allowed address for a PBI device. The S-16 generates the EXTENB signal for all segments of the CPU memory map except:

(a) The Active segments of the O.S. ROM. Any disabled segments of the O.S. ROM generate the EXTENB signal when addressed.

(b) The region occupied by the internal cartridge (if present).

PIN 27 is the External Select (EXTSEL) Input. This input is generated by the (external) decoder resident in the PBI device. This

signal should go low whenever the EXTENB is enabled and the PBI device uses the address generated on the CPU Bus. This input is used to disable the S-16 decoder for the duration of the current bus cycle.

PIN 30 is the RDY input to the S-16. A slow PBI device can extend the CPU bus cycle by pulling this line low when it is addressed.

PIN 40 is the Refresh (REF) output. This output may be used for the refresh timing of volitile memories connected to the PBI.

PIN 1 and PIN 50 are shield grounds.

PIN 41 is Auto-run Present (ARP) pin. This pin goes high whenever an auto-run cartridge is present at the PBI. All auto-run cartridges should pull this line to the "high" state internally.

PIN 42 is Auto-run Disable (ARD) pin. This pin goes high whenever a cartridge is present in the internal cartridge slot. The Auto-run cartridge should disable their decoder whenever this line is in the "high" state.

PIN 43 is Math Pak Disable (MPD) input from the PBI devices. This input is pulled to the "low" state whenever a Parallel Bus Peripheral is selected by the CPU (the enable bit in location D1FDH is set).

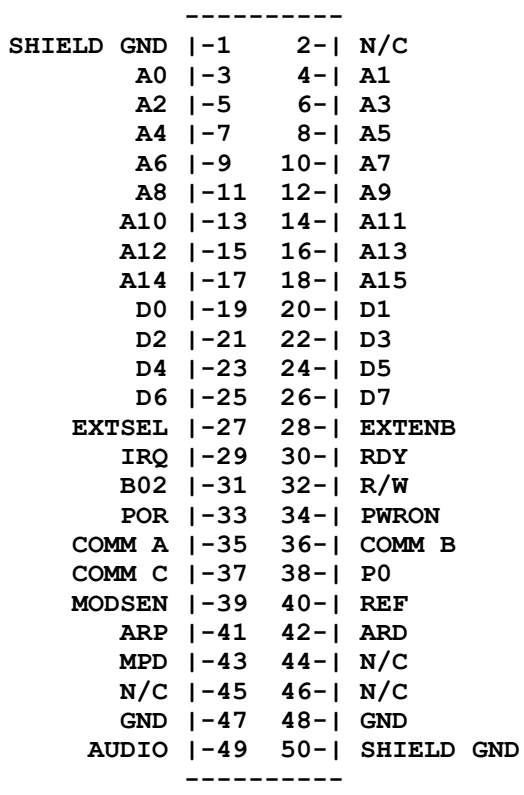


FIGURE 5.2.9 PBI Connector

3.0 Parallel Bus Devices

The Parallel bus will support 3 types of devices:

3.1 Auto-Run Cartridges:

These cartridges are functionally identical to those that plug into the cartridge slot of the S-16 except that they can be up to 32K Bytes in size (in 4K Byte increments). The top address for these cartridges must be BFFFH and they must assert the "AUTO-RUN PRESENT" line when inserted into the expansion box. The auto-run cartridges work under the following constraints:

(a) Only one such cartridge will work at a time.

(b) If a cartridge is present in the internal cartridge slot, the auto-run cartridge is ignored by the S-16.

(c) If no cartridge is present in the internal cartridge slot the auto-run cartridges operate in a manner identical to the cartridge slot cartridges. No additional handlers or O.S. changes are needed.

(d) If an auto-run cartridge is present in the expansion slot, any "External Application" cartridges (See Sec. 3.3) plugged into the Expansion box will be disabled.

(e) The Auto-run cartridges conform to the EXTSEL/EXTENB protocol (have their own decoder).

(f) The Auto-run cartridges must disable their decoder if the "Auto-run Disable" output of the S-16 is active.

3.2 Parallel Bus Peripherals (PBPs)

The PBPs have the following characteristics:

(a) They interface to the S-16 through a well defined handler/O.S. interface. The code for this interface is resident in CPU memory location D600H to D7FFH (COMM A & COMM B areas). The ROM containing this code is physically located on the expansion box.

The S-16 O.S. can support up to 8 PBPs.

(b) Each PBP has a unique handler that resides in the CPU memory space at locations D800H to DFFFH. The ROM(s) containing the code for these handlers are physically resident on the respective peripheral boards (The memory space occupied by the handlers actually contains the Math-pak within the S-16. The Math-pak is disabled whenever any PBP is enabled. (See (c) below).

(c) Locations D1FDH thru D1FFH (in COMM C space) in the CPU memory map are reserved for passing control information between the S-16 and the PBPs.

Location D1FDH is Slot-Select location with the following bit assignments:

7	6	5	4	3	2	1	0
X	X	X	X	E	I	I	I

E = Enable bit. The S-16 sets this bit to logic 1 whenever the O.S. wishes to communicate with a device in the slot whose I.D. is specified

by III. When the Enable bit is set to logic 1 the S-16 disables the Math-pak and maps the region from D800H to DFFFH to the expansion box. The Enable bit is latched in the expansion box and it must be set to logic "0" to disable the PBPs.

III = SLOT I.D. The S-16 O.S. can support a maximum of 8 PBPs. The slot I.D. is latched in the expansion box and a slot remains selected till a different slot I.D. is generated or the enable bit is set to logic 0.

X = Don't Care.

The Slot I.D. decoder is physically located on the expansion box. location D1FEH is Interrupt vector location with the following bit assignments:

7	6	5	4	3	2	1	0
X	X	X	X	IR	I	I	I

IR = Interrupt Request. This bit, when logic 1, indicates to the S-16 O.S. that a device in the Expansion box has interrupted. When this bit is logic 0, no device in the expansion box has interrupt.

III = is the slot I.D. of the highest priority slot that generates the interrupt. The S-16 O.S. assumes that the slots have fixed priority. The slot with an I.D. of 7 has the highest priority.

X = Don't Care.

The priority encoder is physically located on the expansion box. Location D1FFH is un-encoded interrupt location with the following bit assignments:

7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0

IX (X = 0 to 7): This bit is set to logic 1 whenever a device in slot X generates an interrupt. This bit is cleared by the interrupt servicing routine for the device in slot X.

The un-encoded interrupt location allows an application program to mask the interrupts from the specific slots. With the masking arrangement, an application program may ignore the fixed priority by slots and implement its own priority scheme.

(d) A peripheral handler may respond to address in the region D800H-DFFFH only when the slot in which it resides is selected. Location D800H contains the device I.D. of a PBP. If a slot that contains no peripheral is selected, address D800H should return FFH as data.

The peripheral handlers must conform to the EXTSEL/EXTENB protocol as specified in the S-16 Product Specifications.

(e) A peripheral may respond to address in the region D100H to D1FCH only when the slot in which it resides is selected.

(f) The PBPs will have priority over the SIO peripheral when they are addressed generically.

(g) The data between the S-16 and a PBP is passed under control of the peripheral handler for the PBPs.

(h) The PBPs will work if an auto-run cartridge or an internal cartridge is present in the system.

3.3 "External Application" Cartridges:

The External Application Cartridge are a generalization of the auto-run cartridges and the PBPs. They have the following characteristics:

(a) An "External Applications" Cartridge (EAC) can reside at any or all of the address in the region 4000H to BFFFH. They may respond to these addresses only when "opened".

(b) The EACs must be "opened" by the S-16 through the slot select location in the same way as the PBPs.

(c) The EACs must conform to the EXTENB/EXTSEL protocol.

(d) The EACs must have a "handler" (resident in locations D800H to DFFFH) that controls their operation. The EACs must conform to conditions (d) and (e) of section 3.2 above.

(e) The EACs will work only if no auto-run cartridge is enabled in the expansion box. The EACs must input the AUTO-RUN DISABLE line to ascertain that the Auto-run cartridge is disabled before asserting themselves on the Expansion Bus.

(f) The EACs may work even if a cartridge is present in the internal cartridge slot.

4.0 assumptions

(a) The above description of the PBI devices assumes that there is a mechanism in the Expansion Box that prevents more than one auto-run cartridge from being turned on at a time on the PBI. This mechanism may be a daisy chain priority scheme by slots or the auto-run cartridges may be specified to work in only one of the 8 possible slots.

(b) The above description also assumes that there is a power shut-off interlock switch on the internal cartridge door.